IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

LÜPPERT et al

Serial No. 10/628,578

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Atty. Ref.: 1410-794

Group: 2128

Examiner: Phan, Thai Q

For: SYMBOLIC ANALYSIS OF ELECTRICAL CIRCUITS FOR APPLICATION IN TELECOMMUNICATIONS

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February 28, 2006

Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal. The review is requested for the reason(s) stated on the attached sheet(s).

Claims 1-7, 15-27 and 35-40 stand rejected under 35 USC §103(a) as being unpatentable over U.S. Patent 6,134,513 to Gopal in view of U.S. Patent 6,871,334 to Mabuchi et al. All prior art rejections were respectfully traversed and review is sought for at least the following reasons.

Independent Claims 1 and 21

Applicants' independent claims 1 and 21 require generating an admittance matrix for an electrical circuit which is being analyzed, the admittance matrix including *symbolic expressions rather than numerical expressions for at least some* ***components of the electrical circuit***. Further, Applicants' independent claims 1 and 21 require certain steps for solving the equation system for analyzing an electrical circuit, i.e.,

(a) rearranging equations in the equation system;

(b) partitioning the admittance matrix into partitions;

(c) generating a simplified equation system based on the partitioning of step (b).

Referring specifically to Column 5, lines 55-65 of U.S. Patent 6,134,513 to Gopal, the Office Action alleges that the method of Gopal includes generating an admittance matrix including symbolic expressions for at least some *circuit components*. Yet the symbolic names employed by Gopal in the cited passage are only *node names*, i.e., node names expressed in symbolic nomenclature. Symbolic node names are *not* the same as circuit components of an electric circuit in that, e.g., per se they have no particular active influence (capacitance, resistance, inductance, etc.). Labelling the node voltages and the branch currents, symbolically or otherwise, should not be confused with and is not the same as assigning symbolic values to circuit components.

Nor does U.S. Patent 6,134,513 to Gopal teach or suggest Applicants' claimed steps as listed above. For example, Gopal does not rearrange equations having circuit elements symbolically expressed in an equation system. Nor (as properly admitted by the Office Action) does Gopal partition the admittance matrix into partitions and generate a simplified equation system based on the partitioning.

The Office Action attempts to remedies the deficiencies of Gopal with respect to Applicants' "step" limitations by combining Gopal with U.S. Patent 6,871,334 to Mabuchi et al. Mabutchi addresses a peculiar problem of suppressing Electro Magnetic Interference at a design stage of a product, and toward this end employs *numerical* methods to process an equivalent electrical circuit.

In Mabuchi (*see* col. 8, lines 40-54), the current and nodal voltage vectors are divided into parts related to internal and external nodes. Accordingly, the Admittance Matrix is divided into four partial matrices (block matrices). By contrast, Applicants not only split elements of current and voltage nodes vectors, but also elements within the Admittance Matrix are rearranged (e.g., permutated). Mabuchi does not teach or suggest, among other things, Applicants' claimed rearranging of equations in the equation system, i.e., the rearranging of elements within the admittance matrix, particularly such rearranging in an admittance matrix wherein circuit elements are symbolically expressed.

Even if U.S. Patent 6,871,334 to Mabuchi et al. were to teach a rearranging (which it does not), rearranging or manipulation of numerical matrices/arrays is vastly different in nature and extent than arranging or manipulating symbolic data (e.g., of circuit elements). Working with symbolic data rather than just pure numerical data involves considerably different processing/programming ramifications, including memory/working space, program efficiency, and potential crashing program due to excessive and unnecessary symbolic computations. Applicants' claim limitations of rearranging equations, partitioning equations, etc., cannot follow or flow from the teachings of U.S. Patent 6,871,334 to Mabuchi et al..

By contrast, Applicants' rearranging of equations permits a separation of numerical and symbolic variables, e.g., the numerical variables are separated from symbolic variables and the symbolic variables are moved to a remaining bloc for further processing. This rearranging and partitioning allows not only sorting out uninterested nodes but also keeping the dimension of matrix containing symbolic values to a manageable size. This requirement is reflected, e.g., by limitations in dependent claims such as dependent claims 6 and 26, which specifically state that Applicants' step (a) of

rearranging the equations in the equation system is performed in accordance with an identification of interesting nodes for analysis.

In view of the foregoing, the combination of Gopal and Mabuchi lacks, among other things, the teaching or suggestion of using symbolic expressions rather than numerical expressions for at least some components of the electrical circuit in an admittance matrix, as well as the step of rearranging the equations in the equation system and the partitioning.

Various other dependent claims dependent upon independent claims 1 and 21 have further patentable merit. For example, with respect to dependent claims 2 – 3 and 22 – 23, Gopal does not disclose a system for optimizing a component and perturbation/sensitivity analysis. For example, Gopal does not disclose a system involving telecommunication components e.g. discrete-time components and components resulting in asymmetric Admittance Matrix.

Independent Claims 15 and 35

Applicants' independent claims 15 (computer program product) and 35 (method) specify that plural types of connectivity blocks are inserted into the admittance matrix so that differing types of connectivity blocks are symmetric with respect to one another across the main diagonal of the admittance matrix. These and other limitations of independent claims 15 and 35 are not taught or suggested by U.S. Patent 6,134,513 to Gopal. For example, independent claim 15 and 35 specify, e.g., steps for generating an admittance matrix, including, e.g., :

> generating a main circuit admittance block for a main circuit comprising the electrical circuit which is being analyzed;
>
> generating a subcircuit admittance block for a subcircuit comprising the electrical circuit which is being analyzed;
>
> inserting the main circuit admittance block and the subcircuit admittance block on a main diagonal of the admittance matrix;

generating plural types of connectivity blocks which represent connectivity between the main circuit and the subcircuit;

inserting the plural types of connectivity blocks so that differing types of connectivity blocks are symmetric with respect to one another across the main diagonal of the admittance matrix;

using the admittance matrix for analyzing at least a part of the electrical circuit

U.S. Patent 6,134,513 to Gopal does not disclose an Admittance Matrix for a plurality of subcircuits. Fig 15 of Gopal illustrates how the Gopal Admittance Matrix is assembled. There is no teaching or suggestion of subcircuits. Even if a Gopal's "macro" were somehow construed as claimed subcircuit, Gopal does not explain where the macro is stenciled. The fact that Gopal's matrix is symmetric about its diagonal (col. 10, line 27 – 28) does not specify where Gopal places such a macro or any other element. Nor is there any hint that Gopal generates anything even akin to connectivity blocks which represent connectivity between a main circuit and a subcircuit. Indeed the spotty nature of Gopal's matrix and eagerness to eliminate entries confirms that Gopal has no such connectivity block entries. Certainly there is no teaching or suggestion that Gopal inserts anything like differing types of connectivity blocks symmetrically across a main diagonal of the Gopal matrix, particularly since Gopal seems to use only a lower triangle portion of his matrix anyway (see col. 10, line 27 – 31).

Neither Gopal nor U.S. Mabuchi mention connectivity between a main circuit and a subcircuit, much less different types of connectivity blocks as required by Applicants' independent claims 15 and 35.

U.S. Patent 6,871,334 to Mabuchi et al. does not remedy the deficiencies of Gopal. The particular columns of Mabuchi noted in the office action, e.g., columns 8, 9, and 10) merely describe how an arbitrarily defined network can be isolated from the Admittance Matrix. Equation 17 of Mabuchi summarizes the properties of such defined network. Mabuchi has no teaching or suggestion of several networks, nor is there any mention at all of different types of connectivity blocks as required by independent claims 15 and 35.

Dependent claims

Only selected aspects of Applicants' independent claim have been discussed above. Numerous ones of Applicants dependent claims have separate patentable merit. For example, dependent claims 3, 10, 20, 23, 30, and 40 specify that the electrical circuit has a telecommunications component including one of a multi-winded transformer, a loading coil, a line-driver, an analogue cable, and a filter. By contrast, Gopal refers exclusively to resistors, i.e., to the resistive network (associated with power distribution system). As such, Gopal's matrix must be symmetric. Applicants' solution allows inclusion of arbitrary electrical components such as e.g. transformers resulting in krakovians with arbitrary structure. This is exemplified in Applicants' Fig. 6 and Fig. 13.

For reasons including but not limited to the foregoing, Applicants respectfully submit that the Examiner has erred: the rejections should be withdrawn.

Respectfully submitted,
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